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13.5 A Zero-IF Single-Chip Transceiver for up to 22Mb/s QPSK 802.11b Wireless LAN

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Until recently, a 2.45GHz wireless LAN transceiver used the super-heterodyne architecture with an IF of a few 100MHz. This architecture often uses three external filters with accompanying matching networks, two cascaded power amplifiers, (partly) external VCOs and synthesizers, which occupy space and generate extra cost. This direct conversion architecture for IEEE802.11b pushes the level of integration higher by using only one external front-end filter, one power amplifier, a base-band chip, one crystal, a battery and this chip. The block diagram is shown in Figure 13.5.1. The chip is implemented in the Philips 0.5 μ m QUBIC3 BiCMOS process with 34GHz peak f_T and housed in an LQFP 48 package.

A differential LNA is used to reduce LO-RF feed-through and switching noise from digital circuits. The two LNA gain modes (Figure 13.5.2) use two differential pairs (transistor T_1 , T_2 for high gain and T_3 , T_4 for low gain). Shunt feedback improves linearity and process variation immunity. Capacitors C_b are added to the buffer stage built around T_{11} and T_{12} to make it push-pull with better linearity. To improve IP2, make a level shift and to set the transconductance of the mixer in noise-free manner, capacitors C_k are inserted. Only the I mixer half is drawn in Figure 13.5.2 because the Q mixer is identical. The mixer is DC coupled to the active fifth-order opamp-RC Chebychev filter shown in Figure 13.5.3. In Figure 13.5.4 the measured filter transfer function is shown. The filter tuning is by binary switching of unit capacitors in the filter capacitor banks. A tuner determines the optimum tuning bits by measuring the RC time constant using a reference clock signal [1]. The interface between mixer and filter is current-driven. This can be done because the filter node impedance is kept low due to the combination of a large filter capacitor at the input stage and the high cut-off frequency of 7MHz. A pre-filter VGA can be omitted because switches S_1 to S_3 (Figure 13.5.3), lower the gain for strong in-band signals [2]. The unity-gain frequency of the first filter opamp is about 1GHz to keep linearity for high frequencies and immunity for process spreads to the filter transfer function high. Simulated input-referred filter noise is 38nA and kept low by the high filter gain and large filter capacitors. Measured DC offset at the output of the filter at maximum gain is about 60mV, which is low due to good matching and low LO-RF feed-through. An AC coupling succeeds the filter with a controllable high-pass corner. The following variable-gain amplifier (VGA) has 40dB gain in 2dB steps and is connected to the second AC coupling and the driver circuit, which has two gain settings, 1dB apart. The filter capacitors and resistors as well as the resistors in the VGA and driver within I and Q paths are interleaved to keep gain and phase mismatch low. The resulting residual side-band suppression is -32dB. At the input of the driver circuit, the signal is passed to a limiter and Received Signal Strength Indicator (RSSI) circuit, a third-order low-pass Bessel filter and an ADC to allow the state machine to determine the signal strength. Because of the QPSK signal not having a constant envelope, the RSSI level is difficult to estimate accurately. By taking both I and Q signals, using a higher-order low-overshoot RSSI low-pass filter and a reduced limiter/RSSI range (about 30dB), the signal strength can be determined more accurately. Because of the reduced RSSI range, the settling has to be done in at least 3 steps. The measurement of the automatic signal settling for a sinusoidal input is depicted in Figure 13.5.5. After the AGC reset pulse, it takes 9 μ s to determine the correct gain setting and additional 5 μ s

to let the DC offset decay. To speed up DC settling after a gain change, a 10MHz, 1MHz, 100kHz and 10kHz high-pass corner point setting is sequentially used, with suitable time intervals.

At maximum gain, the receiver noise figure is 5.4dB, the input IP3 using 13 and 23MHz offset interfering tones is -4dBm and the input IP2 is +44dBm for 21 and 23MHz offset tones. At -45dBm desired input signal level, an on-off keyed sinusoidal interferer at 25MHz offset from the desired signal can be made up to -6dBm with desired signal gain modulation <10%. The LO leakage at the input of the LNA is -74.5dBm. The receiver has 92dB voltage gain and draws 87mA current from a 3V supply.

The I/Q base-band signal can be applied either as an analog input current or as a digital I/Q bit-stream of 2x11Mb/s. A power-ramp circuit with -1 μ s ramp up/down time reduces the spectral regrowth during transmit start and stop transients. In digital mode, four times over-sampling is used for an on-chip digital filter. Fourth-order time-continuous Butterworth interpolation filters reduce out-of-band spectral emissions. A VGA is merged with the pulse-shaping filters to cover an 8dB range in 1dB steps. The succeeding I/Q modulator with an 8dB gain step converts the base-band signal up directly to RF. A 0dBm and a +5dBm driver deliver the transmit output. The +5dBm driver is differential, to reduce the ground-bounce which can pull the on-chip VCO. A base-band VGA can be made more linear and with a lower power consumption than one at RF. However, the LO suppression would also decrease for low-gain settings. To guarantee sufficient LO suppression, a self-calibration loop is added, and is soon to be tested. It consists of a RF peak detector circuit, I/Q offset DACs at the input of the power ramping circuit and a state machine. Without calibration, LO suppression ranges from 29 to 34dB, depending on the gain setting. The transmitter uses 77mA for 0dBm and 129mA for +5dBm. In the transmit output spectrum shown in Figure 13.5.6, the ACPR is -56dB.

A fully-on-chip VCO with guaranteed tuning range between 1.2 and 1.25GHz is doubled to generate the 2.45GHz LO signal. A half LO frequency VCO is chosen to minimize VCO pulling by the transmit output stages while still maintaining a good tuning range with on-chip varicaps. The VCO phase noise after the doubler is -107dBc/Hz at 1MHz offset. An off-chip loop filter is driven by the fractional-n synthesizer, which gets its reference from a 44MHz crystal oscillator. Two 2.5GHz RC phase shifters are placed close to the Rx and Tx mixers.

The chip micrograph is shown in Figure 13.5.7.

Acknowledgements:

The authors thank T. Framhein for layout, R. Gaethke for the synthesizer, Y. Dufour for the VCO work, P. Caen for design support, Y. Zhang for system support and K. Kimyacioglu for enabling and guiding the project.

References:

- [1] A. Durham et al., "High-Linearity Continuous-Time Filter in 5-V VLSI CMOS", *IEEE J. Solid-State Circuits*, vol. 27, pp. 1270-1276, Sept. 1992.
- [2] A. Pärssinen, et al., "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications", *IEEE J. Solid-State Circuits*, vol. 34, pp. 1893-1903, Dec. 1999.

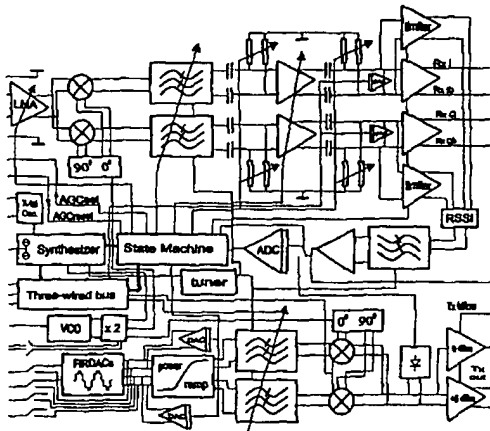


Figure 13.5.1: Block diagram.

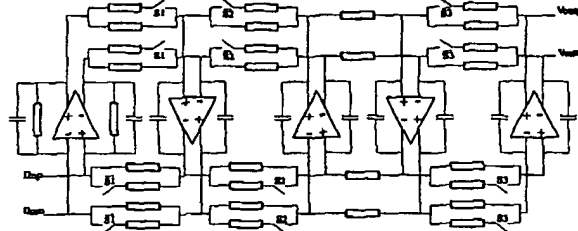


Figure 13.5.3: Receive filter (I channel only).

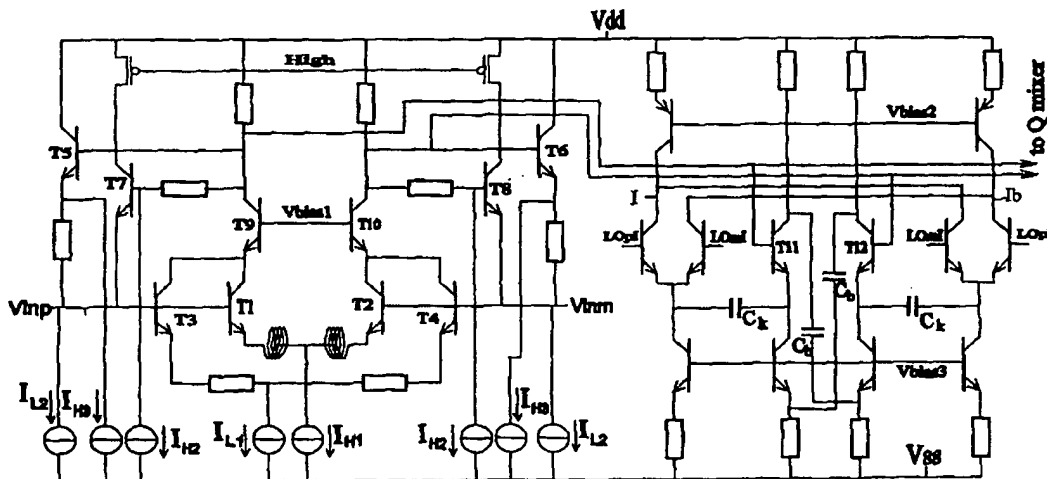


Figure 13.5.2: LNA and receive mixer.

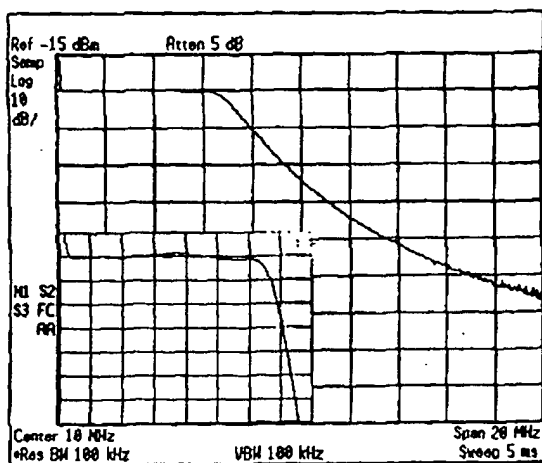


Figure 13.5.4: Receive filter transfer function measurement (line scale: 1MHz & 1dB/div.).

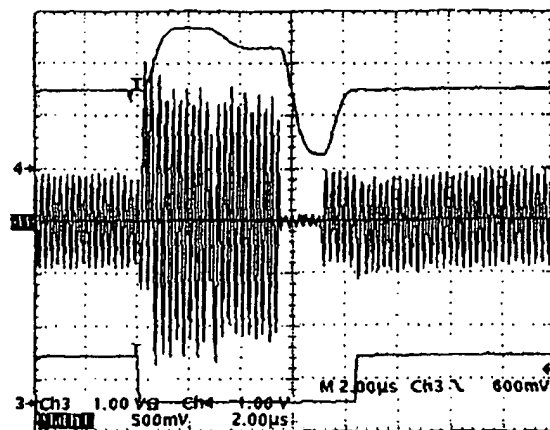


Figure 13.5.5: RSSI voltage, Rx output voltage and AGC reset pulse.

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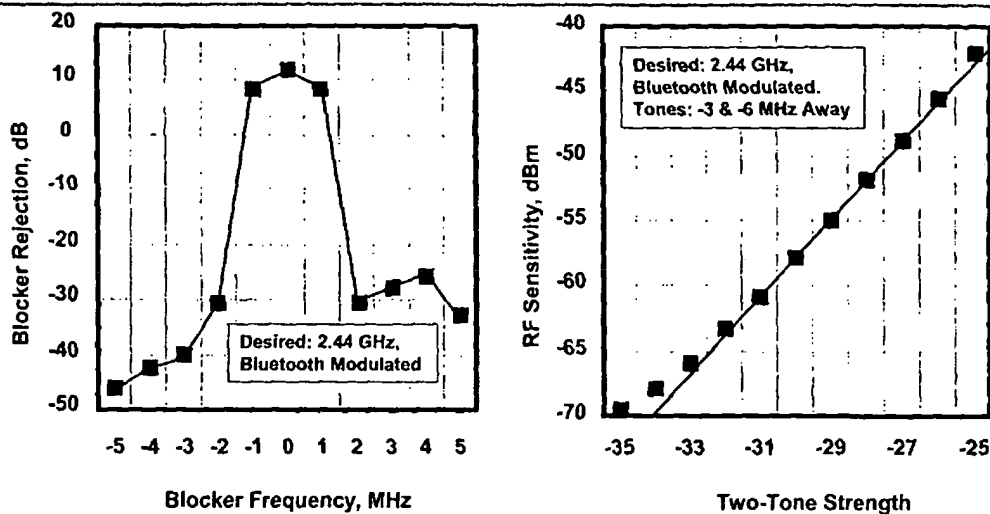


Figure 13.3.6: (a) Receiver in-band blocker rejection; (b) Receiver sensitivity at the presence of a two-tone blocker.

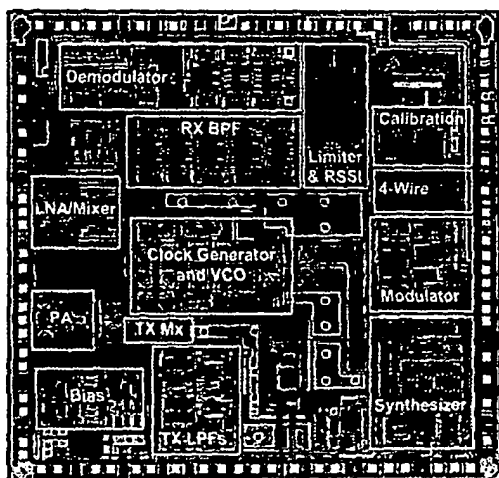


Figure 13.3.7: Chip micrograph.

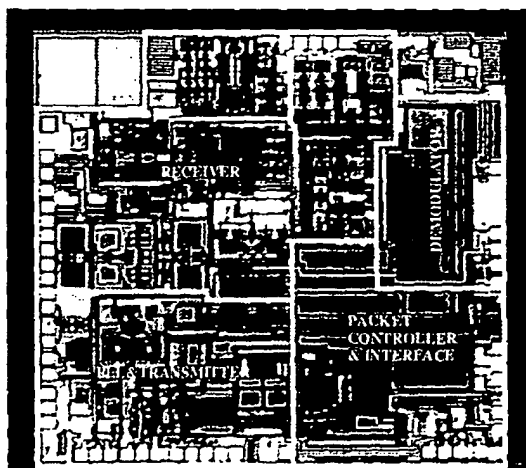


Figure 13.4.7: Die micrograph.

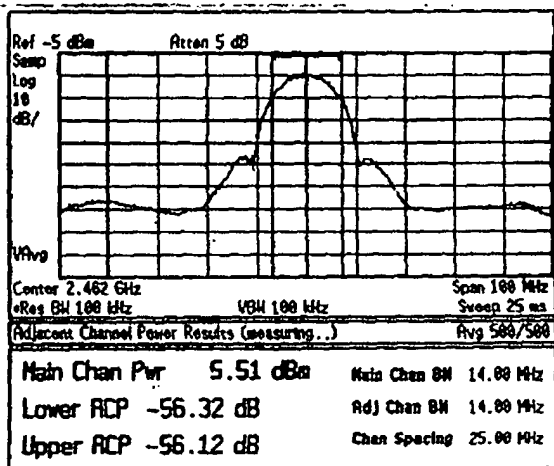


Figure 13.5.6: Transmit output spectrum.

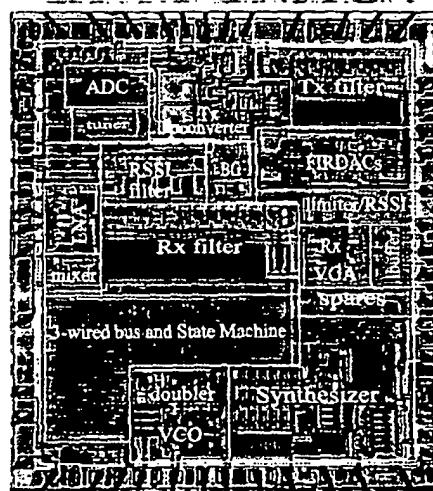


Fig. 13.5.7: Chip micrograph.